TRIP_T Test Board Interface With ASIC Tester

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Introduction

This document describes the signals used for commands and data exchanges between the TRIP_T test board and the ASIC Tester. The following lines of ASIC Tester are used by TRIP_T test board (see also the test board schematic).

1. DCOUT(7 down to 0).
2. DCIN(5 down to 0).
3. PULSE(15 down to 0).
4. ADCIN(3 down to 0).
5. FIFO1(7 down to 0), FIFO2(7 down to 0), FIFO1_STB, FIFO2_STB.

Functions implemented using DCOUT lines

The following are the proposed assignments for DCOUT lines. They are passed through FPGA without changes. It was agreed that TRIP_T programmable interface is not implemented inside the FPGA.

DCOUT(7) = TRIP_T programmable interface RESET.
DCOUT(6) = power on/off command.
DCOUT(5) = TRIP_T programmable interface CONTROL.
DCOUT(4) = TRIP_T programmable interface CLOCK.
DCOUT(3) = TRIP_T programmable interface DATA_IN.
DCOUT(2) = TRIP_T voltage pin reading MUX_EN.
DCOUT(1) = TRIP_T voltage pin reading MUX_SEL_1.
DCOUT(0) = TRIP_T voltage pin reading MUX_SEL_0.

Functions implemented using DCIN lines

DCIN(0) = TRIP_T digital current supply too HIGH.
DCIN(1) = TRIP_T digital current supply too LOW.

DCIN(2) = TRIP_T analog current supply too HIGH.
DCIN(3) = TRIP_T analog current supply too LOW.
DCIN(4) = TRIP_T programmable interface DATA_OUT.
DCIN(5) = FPGA busy status bit.

Functions implemented using ADCIN lines

ADCIN(0) = TRIP_T analog current supply.
ADCIN(1) = TRIP_T digital current supply.
ADCIN(2) = TRIP_T multiplexed output for reading one of the four voltages on PIN41, 42, 51 or 52, as selected by DCOUT(1 to 0) settings.
ADCIN(3) = TRIP_T reading of PIN53=INJECT.

Functions implemented using FIFO lines

The two ASIC Tester's FIFO are used to readout miscellaneous information like the 16bit discriminator outputs of TRIP_T or the digitized analog output of TRIP_T.

Functions implemented using PULSE lines

The ASIC Tester's PULSE lines are the main lines used for miscellaneous test implementation.

The desired test is configured using four eight bit registers. The register data is set using PULSE(0 to 7) while the register's address is set using PULSE(8 to 10). A positive strobe on PULSE(15) is used to register the register's address and data information

The TRIP_T testing is based on a sequencer machine implemented inside the FPGA. The sequencer is started by a positive strobe on PULSE(14). It contains two phases. The first phase puts TRIP_T in acquire mode, the second in read out and digitize mode.

While in acquire phase, a programmable number of PIPECLK are issued (see Register 0x04 below). The PIPECLK signal has 50% duty cycle with 320ns period. A charge injection can take place anywhere inside this phase with parameters set by Registers 0x01, 0x02 and 0x03. We can inject using the IJNECT pin or directly the even and/or odd TRIP_T inputs. The injection moment is in 10ns time increments and the charge injected can have a maximum of four predefined values.

While in readout mode the analog outputs of the TRIP_T (pulse amplitude and time) are digitized and stored inside FPGA BRAM. This phase is a fixed signal pattern. It consists basically of four SKIPB, which allow the readout of four consecutive pipeline cells.

To transfer the data stored in FPGA BRAM to ASIC Tester FIFO a positive strobe on PULSE(13) must be issued. The BRAM data to be transferred (discriminator or analog output information) is set using Register 0x04.

PULSE(0 to 7) = FPGA registers data lines.
PULSE(8 to 10) = FPGA registers address lines.
PULSE(11) = not used.
PULSE(12) = FPGA reset.
PULSE(13) = dump FPGA RAMB into ASIC Tester's FIFO.
PULSE(14) = FPGA TRIP_T sequencer start.
PULSE(15) = FPGA registers strobe pulse.

Register address 0x01. This register's data contains the pipeline clock number (from the acquire phase of the sequencer) at which an injection takes place.

Bit7 = not used.
Bit6 = injection pipeline clock number bit 5 MSB.
Bit5 = injection pipeline clock number bit 4.
Bit4 = injection pipeline clock number bit 3.
Bit3 = injection pipeline clock number bit 2.
Bit2 = injection pipeline clock number bit 1.
Bit1 = injection pipeline clock number bit 0 LSB
Bit0 = '0' injection when pipeline LOW, '1' injection when pipeline HIGH.

Register address 0x02. This register's data contains the time position within a pipeline clock (as defined by Register 0x01) when the injection occurs as well as where the injection occurs (TRIP_T pin#39 or even /odd inputs).

Bit7 = not used.
Bit6 = '1' enable injection, '0' disable injection on TRIP_T pin#39.
Bit5 = '1' enable injection, '0' disable injection on TRIP_T even inputs.
Bit4 = '1' enable injection, '0' disable injection on TRIP_T odd inputs.
Bit3 = clock number bit 3 MSB.
Bit2 = clock number bit 2.
Bit1 = clock number bit 1.
Bit0 = clock number bit 0 LSB.

Register address 0x03. This register's data contains the binary encoded charge that we want to be injected, according with settings defined by Register 0x01 and 0x02.

Bit7 = not used.
Bit6 = not used.
Bit5 = not used.
Bit4 = not used.
Bit3 = not used.
Bit2 = not used.
Bit1 = Charge code number bit 1 MSB.
Bit0 = Charge code number bit 0 LSB.

Register address 0x04. This register's data contains the number of TRIP_T pipeline clocks to be issued during the acquire phase of the sequencer. The bits used are 5 down to 0.

This register's data contains also (see bit 7 and 6) the FPGA BRAM we want to transfer to ASIC Tester FIFO when a strobe of PULSE(13) is issued: '00' for discriminator data BRAM, '01' and '10' for first and second BRAM with analog output data.

Bit7 = code number bit 1 MSB to transfer BRAM to ASIC FIFO.
Bit6 = code number bit 0 LSB to transfer BRAM to ASIC FIFO.
Bit5 = pipeline clock number bit 5 MSB.
Bit4 = pipeline clock number bit 4.
Bit3 = pipeline clock number bit 3.
Bit2 = pipeline clock number bit 2.
Bit1 = pipeline clock number bit 1.
Bit0 = pipeline clock number bit 0 LSB.

Simulation waveforms

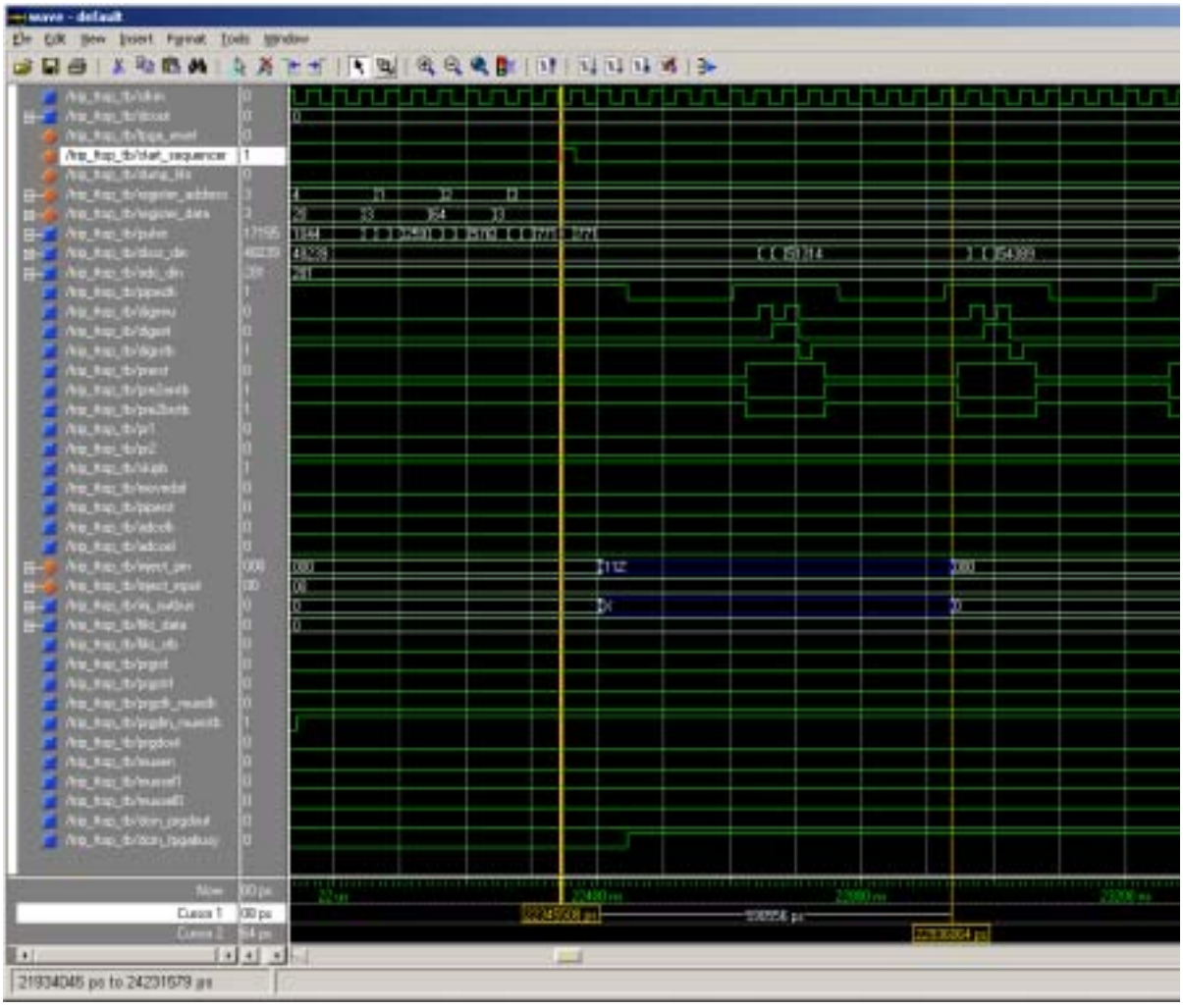

Figure 1 Sequencer start.

According to simulation example presented in Figure 2 the sequencer's parameters are defined as:

1. A decimal value of 20 in Register 0x04 means that 21 low cycles of PIPECLK will be issued during the acquire phase. Note: if zero is written, one PIPECLK will be issued.
2. A decimal value of 3 in Register 0x01 means that the injection will occurs when PIPECLK number is 1 and the PIPECLK is high.
3. A decimal value of 64 (or binary 0100.0000) in Register 0x02 means that the injection point is on the INJECT pin and the CLK number is zero (range 0 to 15).
4. A decimal value of 3 in Register 0x03 means that the charge to be injected has the code number 3. In particular that means "11Z" on the inject bus.
5. After the above parameters were defined, the START_SEQUENCER command is sent (see first highlighted cursor).
6. A burst of 20 PIPECLK cycles follows (only first two shown). During each PIPECLK=HIGH phase, the discriminator enable lines are toggled and three 16bit words will be stored in a BRAM: the upper 16 discriminators, the lower 16 and the pipeline cell ID.

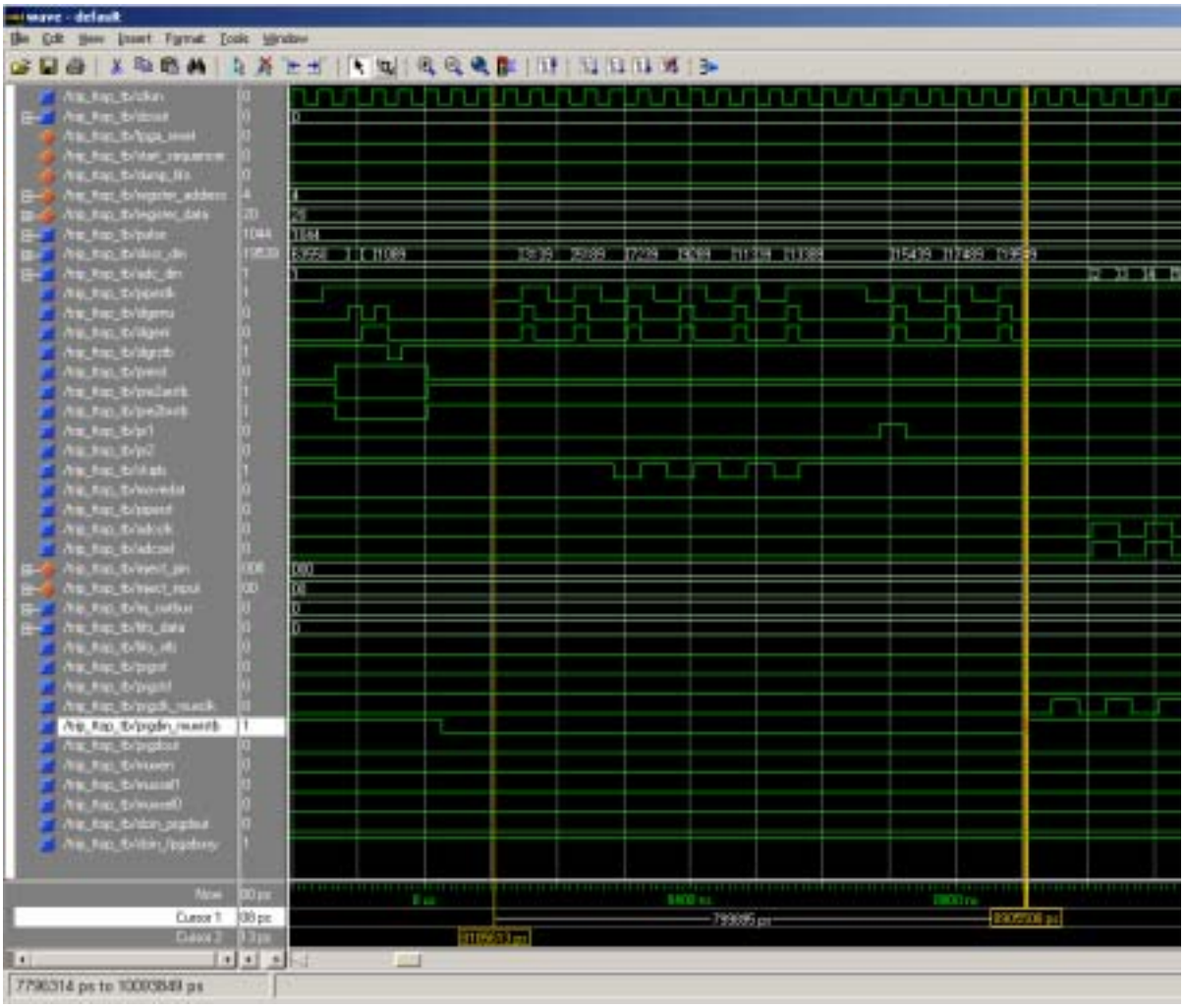

Figure 2 End of acquire phase and beginning of readout phase.

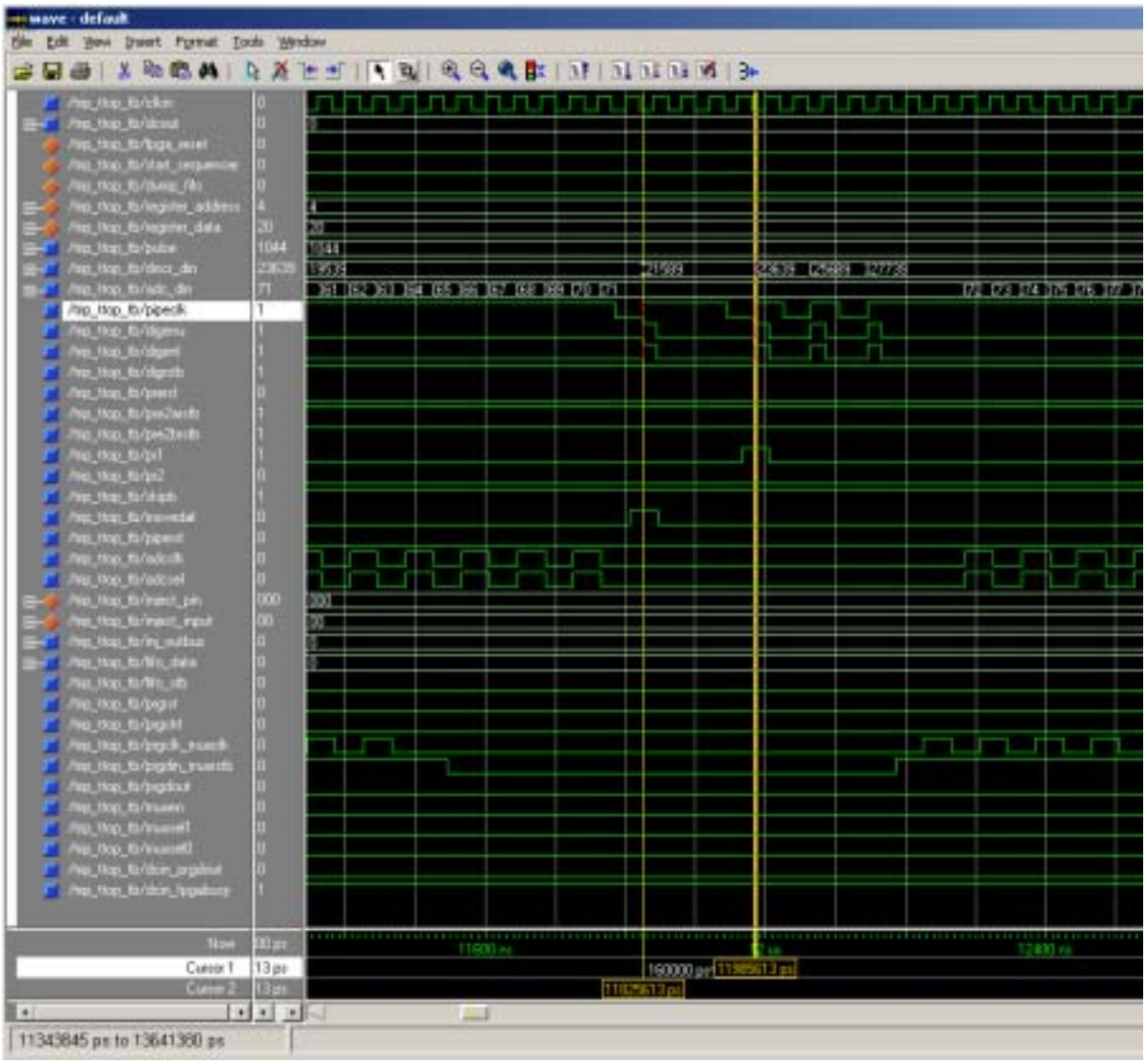

Figure 3 End of one SKIPB associated readout and beginning of the next one.

7. At the end of the sequencer's acquire phase (see last PIPECLK in Figure 2) the readout phase starts by itself. It contains a header of four SKIPB triggers (L1A) followed by the readout of all four hit values (if any) to which the four triggers pointed to.
8. Figure 2 shows also the beginning of the ADC part of the readout phase. The digitization of hit's amplitude and time analog signal will take place for all 32 channels (see ADCCLK signal). The 10 bit ADC word of analog TRIP_T outputs is concatenated with the six MSB of discriminator outputs (i.e. the pipeline cell ID) and stored as a 16 bit word in a BRAM for further download to ASIC Tester's FIFO.
9. Figure 3 shows the end of the readout associated with the first SKIPB trigger and the beginning of the readout associated with the second SKIPB trigger. The chaining of

MOVEDATA and PR1 signals can be seen. To store the information from all four SKIPB we used two FPGA BRAM.

10. When all four SKIPB triggers are readout in BRAM, the sequencer cycle is finished and the FPGA is available for other ASIC Tester's commands. See signal DCIN_FPGABUSY going low in Figure 4.
11. Finally the transfer of the desired BRAM data into ASIC Tester FIFO can be started, as seen in Figure 4. First the BRAM code number is written in Register 0x04 and then the DUMP_FIFO command is issued.
12. The sequencer's full cycle is 2064 FPGA clock ticks. For the external 26MHz crystal used, the FPGA internal clock is 104MHz thus the sequencer's full cycle is ~20micro sec. The download of one BRAM to ASIC FIFO is 514 FPGA clock ticks or ~5micro sec (at a 52MHz FIFO clock rate).

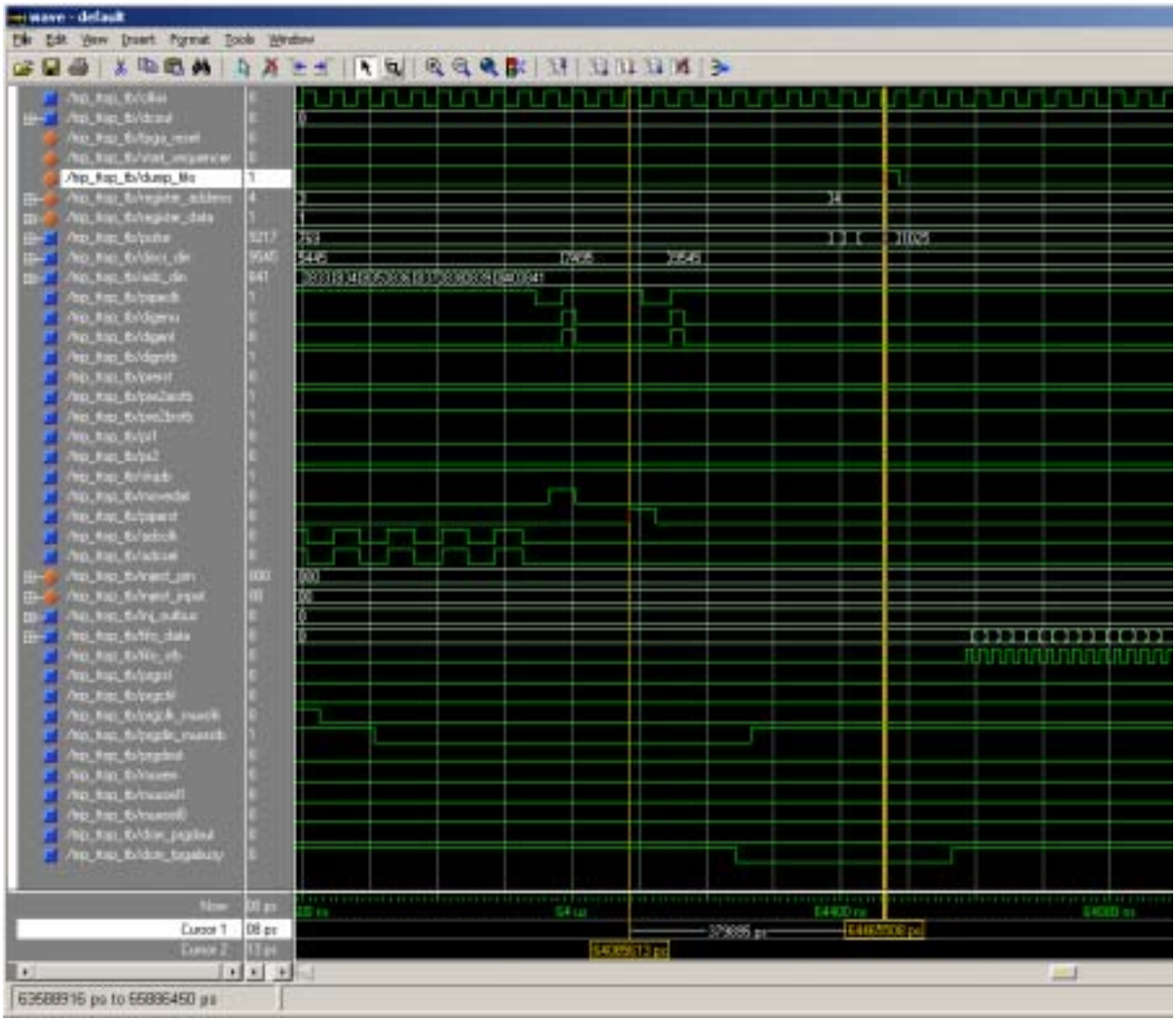

Figure 4 End of one sequencer cycle and begin of data transfer to ASIC FIFO.